

### **Remarks**

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated April 20, 2005, indicated that claims 1-9 are rejected under 35 U.S.C. § 103(a) over Larky *et al.* (U.S. Patent No. 6,311,294) in view of Thomson (U.S. Patent No. 6,073,205).

Applicant respectfully maintains the traversal of the Section 103(a) rejection because the Office Action relies on a combination of references that are unrelated to each other and the claimed invention. Thus, the Office Action fails to present the requisite evidence of correspondence and evidence of motivation to support the asserted modification.

The primary '294 reference is directed to a method of sending bulk data in response to a device 14 sending a positive (data available) acknowledge signal to a host 12. *See* column 6, lines 1-12. The Office Action acknowledges at page 3 that the '294 reference fails to teach a FIFO in connection with this bulk data transfer. The '294 reference also fails to teach a situation where the FIFO buffer is empty as well as a bus interface sending an interrupt to the processor in response to selected ones of the requests when the buffer is empty and no interrupts have yet been generated since the processor has written into the buffer. In contrast, the '294 reference merely discusses a device sending NAKs once it does not have any more bulk data. The lack of bulk data does not correspond to an empty buffer because though no bulk data is available, there still may be data, just not enough to qualify as "bulk" data. Therefore, the device does not experience the situation of an empty buffer.

Without presenting any evidence or explanation of how the combination would be implemented, the Office Action proposes modifying the '294 device 14 to include a FIFO buffer taught by the '205 reference. The '205 reference, unlike the '294 reference, is directed to individual write requests, not bulk data. The '205 device also fails to teach a situation where the FIFO buffer is empty as well as a bus interface sending an interrupt to the processor in response to selected ones of the requests when the buffer is empty and no

interrupts have yet been generated since the processor has written into the buffer. Thus, the proposed combination still fails to correspond to each of the claimed limitations.

The cited combination of references also fails to teach a first station that repeatedly sends requests for data to a second station and also fails to teach a second station that responds to each request by sending a message with a data item or sending a negative acknowledge signal, as claimed. The Office Action cites portions of the Background section of the '294 disclosure (pending-IN process) as allegedly corresponding to these claimed aspects; however, the '294 disclosure teaches that the cited host 12 and device 14 operate using an alternative process that intentionally avoids these claim limitations and expressly teaches away from the claimed invention. *See* column 5, lines 20-26 and line 67 – column 6, line 12. The relied upon embodiment of the '294 reference does not operate in accordance with the cited teachings of the reference's background section; therefore, the proposed modification (which does not address this deficiency) of the relied upon '294 embodiment fails to correspond to the claimed invention.

Moreover, the Office Action fails to present evidence of correspondence to the claimed bus interface sending an interrupt to the processor in response to selected ones of the requests. While the cited portion of column 4 identifies an interface involved in communication, there is no teaching that a bus interface sends an interrupt to the processor in response to selected ones of the requests. The '294 reference teaches that the device 14 only sends a NAK or additional data in response to a request from the host 12. *See* column 6, lines 13-32. Thus, the '294 reference fails to teach a bus interface of a second station sending an interrupt to the processor in response to selected ones of the requests. Without a showing of correspondence to each of the claimed limitations, the Section 103(a) rejection cannot be maintained. Applicant accordingly requests that the rejection be withdrawn.

In view of the reliance on the '294 reference's restriction to bulk data transfers, Applicant fails to recognize any evidence that inserting the '205 FIFO buffer into the '294 system would achieve the structure and function of the claimed invention or that the skilled artisan would be motivated to perform the proposed modification. It would be illogical to process bulk data through a FIFO as FIFOs are not large enough to efficiently process bulk data. Without presenting any evidence of motivation in the cited references to modify the

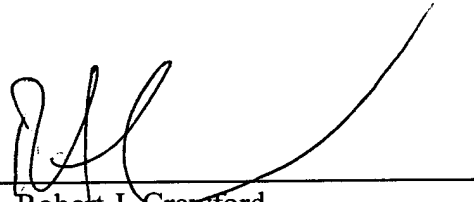
'294 reference to achieve the claimed invention, the Office Action fails to present a *prima facie* Section 103(a) rejection and Applicant requests that the rejection be withdrawn.

Moreover, the primary reference cited by the Office Action teaches away from the claimed invention. The instant invention is directed to, for example, a bus system that includes a first station repeatedly sending requests for data to a second station and the second station responding to each request. *See, e.g.*, claim 1. The Office Action relies on a portion of the Background of the '294 reference (column 2, lines 36-48) as allegedly corresponding to these limitations. The further citation to the Summary (column 3, lines 18-38) teaches that the host 12 only sends IN tokens to the device after receipt of a data available signal, and the device can stop the host's sending of IN tokens by sending a dry signature signal. This ability to prevent the host from sending the IN tokens means that the host does not send the tokens repeatedly, merely upon initiation by the device. As discussed above, the '294 reference thus teaches away from these aspects. The '294 reference teaches an alternative system where the device 14 (alleged second station) initiates bulk data retrieval, which prevents the host 12 (alleged first station) from continuously sending IN tokens to the device 14. *See*, column 5, line 67 – column 6, line 12. The '294 system purposely avoids having the host repeatedly sending requests to the device in order to relieve inefficiencies such as traffic burden on the bus and degradation of overall system performance. *See* column 2, lines 49-62. Since the primary '294 reference teaches away from the claimed invention, the skilled artisan would not be motivated to modify the '294 reference as asserted. Applicant accordingly requests that the rejection be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Mr. Peter Zawilski, of Philips Corporation at (408) 474-9063.

*Please direct all correspondence to:*

Corporate Patent Counsel  
Philips Intellectual Property & Standards  
1109 McKay Drive; Mail Stop SJ41  
San Jose, CA 95131

By:   
Name: Robert J. Crawford  
Reg. No.: 32,122  
(VLSI.412PA)

CUSTOMER NO. 24738